Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: RTL VERIFICATION USING VERILOG (ECE - 4021)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw ROBDD for the synchronous counter that counts in the sequence 0,1,2,4,7,0,…. Show all the steps. Also perform ITE algorithm for the given sequence counter.

1B. Explain ALAP algorithm with an example.

1C. Assume an X FPGA has its technology schematic using only 2:1 multiplexer. Perform technology mapping for a Full subtractor circuit.

(4+3+3)

2A. Apply LIST-L Scheduling algorithm for the given data flow graph shown in **Fig 2A**. Assume γ=4, $M_1=M_2=M_3=M_4=M_5=0$; $M_6=M_7=1$; $M_8=M_9=M_{10}=M_{11}=2$. Draw the scheduled graph under resource constraints.

2B. Determine the prime implicants for the following function using iterated consensus method: $F=\sum m(0,1,6,7,8,9,13,14,15)$

2C. Draw control and data flow graph for a 2-bit comparator.

(4+3+3)

3A. Find the essential prime implicant for the set of prime implicants F(A, B, C, D) = {C_1, C_2, C_3, C_4,C_5} where C_1=B.D, C_2=A.C' , C_3=A'.C, C_4=C'.D , C_5=A'D using ESPRESSO algorithm.

3B. Write the behavioural VHDL code for 55-bit comparator using generics and **for loop** statement

3C. Draw sequencing graph for the following sequential statements x=a*b ; y=c*d ; z=x+y. Apply clique partitioning algorithm, draw conflict graph and determine operation binding resources. The node numbers can be suitably assumed.

(4+3+3)

4A. Write a Verilog-AMS code for the circuit shown in **Fig 4A**, to calculate the voltage across R_L. The values can be suitably assumed.

4B. Write the Verilog AMS code for the given expression to calculate V=I.R. Use parameter declaration. The values can be suitably assumed.

4C. Write the syntax for Parameter declaration and Electrical declaration.

(4+3+3)

5A. Write the structural VHDL code for JK Flip-flop using only NAND gates. Assume NAND gate as the component. Write the program for the entire hierarchy.

5B. Write the sequential VHDL code for 4 bit parallel adder using **for loop** statement.

5C. Write the syntax for with select and when else statement in VHDL. Also state in which modelling "with select" and "when else" statements are being used.

(4+3+3)

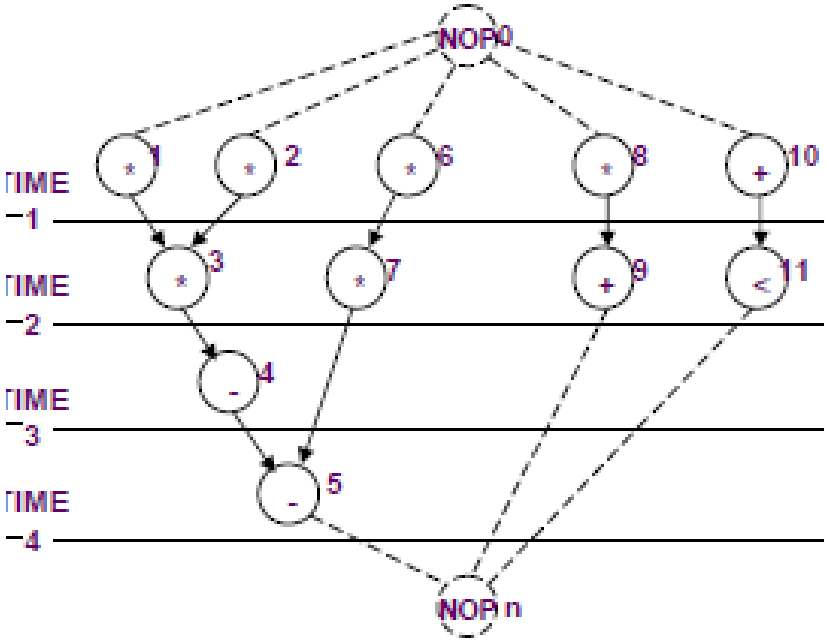

Fig. 2A

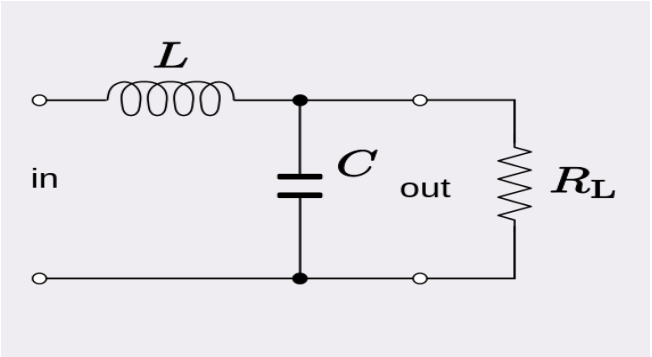

Fig. 4A