Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

MAKEUP EXAMINATIONS, JUNE 2019

COMPUTER ORGANISATION AND MICROPROCESSOR SYSTEMS [ICT 2202]

REVISED CREDIT SYSTEM

(11/06/2019)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Given M = $16_{(10)}$ and Q = $-12_{(10)}$, perform multiplication using Booth's Algorithm indicating all the steps. **5**

1B. If AX = F123H, BX = -81H, what is the content of AX register after the execution of the following instructions: **3**

i. IMUL BX ii. IDIV BL

1C. Explain the function of the following pins of 8086: **2**

i. ALE ii. READY

2A. Explain indirect memory addressing modes of 8086 with an example for each. **5**

2B. Design the processing section of 4x4 Booth's multiplier. **3**

2C. Write an 8086 procedure to interface DC motor to 8086 through 8254. **2**

3A. What is the need of cache memory in computer system? Discuss the following cache mapping techniques: fully associative mapping, direct mapping and set associative mapping. **5**

3B. Write an assembly language program to search for an element 'n' in an array of ten 2 – digit hexadecimal numbers located in the data segment and display the message accordingly. The element 'n' is a 2 – digit hexadecimal number accepted from the keyboard. **3**

3C. Explain the following assembler directives **2**

i. ASSUME ii. ENDS iii. OFFSET iv. DT

4A. Explain the internal architecture of 8259 IC with the help of a neat diagram. Explain how 8259 ICs can be cascaded. **5**

4B. With a neat diagram, explain mode 1 and mode 2 operations of 8255. **3**

4C. Draw the circuit diagram of a 4 – bit combinational shifter that is capable of rotating bits by one, two or three positions to the left. **2**

5A. What are the steps involved while servicing an interrupt? With neat diagrams, explain polled and daisy chain techniques for servicing multiple interrupts. **5**

5B. Explain the concept of memory segmentation in 8086 and its advantages. **3**

5C. Explain the importance of various control flags available in the flag register of 8086 **2**