Reg. No.												

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M. TECH (OPEN ELECTIVE) DEGREE END SEMESTER EXAMINATION APRIL/MAY 2019

SUBJECT: ARM PROCESSOR AND APPLICATIONS (ECE - 5233)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. With schematic diagram, explain how virtual memory address (p, n) is mapped to physical memory address (p', n). Design a memory mapping scheme with the following specifications.

Virtual address space = 64 K words

Main memory size = 16K words

Page size = 2K words

Given : Virtual address issued = 0111100000101011

1B. ARM processor connected to Unified cache of 32KB with aggregate miss rate = 1.99%. Same processor is connected to split cache of 16KB with Instruction miss rate = 0.64% and Data miss rate = 6.47%. Which one is better based on Average Memory Access Time (AMAT)?

Assume: 75% of accesses are instructions.

Hit time = 1

Miss Time = 50.

Data hit has 1 stall for unified cache.

1C. Discuss four major design rules in RISC machines.

(5+3+2)

2A. With block diagram, describe how ARM core is used in VLSI Ruby II Advanced Communication Processor.

2B. ARM state LPC 2129 target board. Write a program to display LEDs is connected to each pins starting from P1.16 to P1.23 of IODIR register. LEDs connected to these pins should be turned on and off one by one with a maximum time delay in between. Repeat the sequence.

2C. What are the different data types ARM supports in high level languages? Explain.

(5+3+2)

3A. Discuss: i) handling of interrupt latency ii) exception priorities

3B. What are the different types of COMPARE and MULTIPLY instructions in ARM? Explain each with one example.

3C. Discuss ARM address register structure.

(5+3+2)

4A. Explain AMBA based system emphasizing on bus transfers, slave, APB, AHB and ARM multiplexed bus scheme.

4B. ARM mode in Thumb state. Write a program to add two 64 bit numbers stored in memory locations pointed by registers r0 and r1. Store the sum in memory location pointed by register r0.

4C. Discuss 4 KB cache direct mapped with all main memory locations which end with 824. Draw necessary sketches. What are limitations of this scheme and how to overcome. Discuss.

(5+3+2)

5A. Sketch block diagram of ARM core data flow model and describe the followings:

i) Barrel Shifter
ii) CPSR
iii) General Purpose Register set

5B. Consider ARM processor is in ARM state. How are stack operations carried out in the processor? Tabulate all the addressing modes and explain with an example.

5C. Explain Interrupt I/O strategy with algorithm or sample program used for implementation.

(5+3+2)