Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (ME) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2019
SUBJECT: LOW POWER VLSI DESIGN (ECE - 5221)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. List the components of dynamic power in VLSI and discuss the major factors affecting the power dissipation in each case.

1B. Explain the dynamic voltage scaling for reduction of power in VLSI with the help of a neat diagram. Also explain the significance of combined scaling of voltage and frequency.

(5+5)

2A. With help of an example discuss how Shannon expansion can be used to implement Dynamic Supply gating? Explain the merits of Dynamic Supply gating.

2B. Discuss i) pre computation and ii) guarded evaluation strategy for reducing the dynamic power in computational blocks with suitable examples.

(5+5)

3A. List and explain the factors that influence the leakage power in MOSFETs.

3B. Explain the advantages and disadvantages of MTCMOS circuits.

3C. Discuss the techniques used for lowering the leakage due to tunnelling.

(4+3+3)

4A. What is the motivation for going for low swing buses? Explain. Also mention its limitations.

4B. What are the techniques employed to reduce the capacitance of interconnects? List and explain.

4C. Why do we make use of copper interconnects in today's VLSI? Give reasons.

(4+3+3)

5A. Explain i) procrastination scheduling and ii) Object code compression technique for system level power reduction.

5B. Describe the fundamental principle of adiabatic switching and the conditions required for proper operation.

5C. Discuss the merits and demerits of predictive technique as a DPM policy.

(4+3+3)