ECE 2152 COMPUTER ORGANIZATION AND ARCHITECTURE (E&C)

Description	Equation
2 gate delays	$C_{i+1} = x_i y_i + x_i c_i + y_i c_i$
3 gate delays	$S_i = x'_i y'_i c_i + x'_i y_i c'_i + x_i y'_i c'_i + x_i y_i c_i$
Generate and propagate terms	$C_{i+1} = X_i Y_i + X_i C_i + Y_i C_i$ $C_{i+1} = G_i + P_i C_i$ Where, $G_i = X_i Y_i$ $P_i = X_i + Y_i$
Delay calculations for the adders	T(n) = (n-2)* (CSA add time) + (CPA add time) T=m*(clock period) +($\log_2$ k)* full adder time
Delay calculations	No. of CSA levels = $[\log_{1.5}(N/2)]$ For 'n' operands can be added in time given as: T(n) = $[\log_{1.5}(n/2)]$ x (CSA add time) + (CPA add time)
Delay calculations for the multipliers	T(n)= (4n-2)⌂
Avg. Access Time	$t_{avg} = ht_c + (1-h)(t_c - t_m)$
Efficiency	$Efficiency = \frac{1}{[1+\gamma(1-h)]}$ Where, $\gamma = \left(\frac{t_m}{t_c}\right)$