Question Paper

Exam Date & Time: 10-Feb-2021 (02:00 PM - 05:15 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

MANIPAL SCHOOL OF INFORMATION SCIENCES, MANIPAL
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN) DEGREE EXAMINATION - FEBRUARY 2021

High Level Digital Design [EDA 601]

Marks: 100 **Duration: 180 mins.**

WEDNESDAY, FEBRUARY 10, 2021

Answer all the questions.

1)	Implement the F = ∑WXYZ(1, 2, 4, 5, 6, 9, 10, 14) logic function using 4x1 multiplexer (TLO-1.1)	(10)
2)	Explain Carry Save Adder with neat diagram. (TLO-3.3)	(10)
3)	Design the 8 bit barrel shifter which can perform5 bit right shift and 2 bit leftshift. (TLO-4.2)	(10)
4)	Write the difference between latch and flip-flop (TLO-6.1)	(10)
5)	Design an single port RAM and explain read and write operation (TLO-6.4)	(10)
6)	Write the difference between Mealy Machine and Moore Machine. (TLO-7.1)	(10)
7)	Explain the following (TLO-8.1) (2*5=10) a. Static Timing Analysis b. Dynamic Timing Analysis	(10)
8)	Design Real Time Clock with following features (TLO-10.1) a. Display - Hr : Min : Sec b. Clock freq 600 KHz	(10)
9)	Design an Asynchronous FIFO (TLO-11.1)	(10)
10)	Briefly explain the early bus termination& locked transfer (TLO-12.1)	(10)

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